MEMO

Date	27/02/2013	**Ref**	TEC-QT/2013/398/CV
From	Carole Villette Tommaso Ghidini	**Visa**	M. Nikulainen
To	Industry, ESA PA Managers	**Copy**	TEC-QTM: G. Corocher, J. Hokka, S. Heltzel, TEC-QTC: L. Marchand TEC-QQ: R. Ciaschi TEC-Q: W. Veith CNES: Th. Battault

Subject: SMT Verification as per ECSS-Q-ST-70-38C, revised work procedure

In order to improve the efficiency and ESA customer service of the ESA SMT verification process per ECSS-Q-ST-70-38C, the following procedure is required for any new or delta SMT verification request from Industry to ESA. This procedure may evolve once the ECSS-Q-ST-70-38C will be updated.

1. A formal request shall be sent by Industry to ESA by an official letter. E-mails or telephone requests shall not be served. Following the request, the verification programme shall be sent by post and uploaded on the SMT server. The verification programme shall contains the information requested in Annex 1.

2. Requests shall be addressed to Carole Villette TEC/QTM (ESTEC, PO Box 299-2200 AG Noordwijk ZH- The Netherlands) with a mandatory copy to T. Ghidini TEC-QTM and to the relevant PA Manager (list enclosed in Annex 2) of the ESA project concerned by the SMT verification.

3. In addition to the requested scope of the technical work, the concerned ESA project and the expected time-line for the delivery of the results shall be indicated. Without a clear indication of an ESA project customer, the SMT verification will not be considered.

4. Furthermore, new or delta verification (eg. Change of soldering machine, solder paste...) shall not be supported by ESA without a specific request from an ESA project PA Manager.

In order to facilitate the review of the verification programme the content of the different documents is Annexed to this letter.

In order to assure the quality of the input to ESA and avoid unnecessary iterations, it is recommended that the microsections are performed in the laboratories listed in Annex 4 or by Industry proposed laboratory that has been accepted by ESA TEC-QTM .

C. Villette
Materials Technology Section

T. Ghidini
Head of Materials Technology Section

Enclosed:

Annex 1: Content of the verification programme to be submitted to ESA
Annex 2: Additional information needed related to the verification programme
Annex3: List of ESA PA Managers with its associated programme
Annex4: List of companies recommended to perform microsections
Annex5: TEC-QT/2012/206/CV
Annex 6: TEC-QT/2010/38/CV

Annex 1

Content of the verification programme to be submitted to ESA

The verification programme shall be delivered to ESA for review and approval. It is also recommended to provide the associated PID with the verification programme. The verification programme shall contain as a minimum the following:

1. Indication of the method of assembly

- Assembly method such as machine reflow (Vapour Phase, convection reflow)
  Note: When machine reflow is used then hand soldering shall also be considered for verification.
- Assembly by hand using a soldering iron
- Assembly using hot air (repair station)
- Statement of compliancy of assembly with respect of the PID

2. PCB information

- PCB material (Polyimide, epoxy, thermount, duroid...)
- Number of layers. A single sided or double sided PCB shall not be considered valid for a verification exercise exception
- Thickness
- Built up with identification of signal and full copper plane
- Location of the devices on the PCB
- Connection of the pads to the internal layer shall be representative of the flight hardware
  - By via in pad
  - By track connected to vias
  - By tracks to other location

  It is recommended to have at least the corner leads (to be microsectioned) connected to the internal layers when applicable
- Location of the mechanical fixation
  - Location of the stiffener
  - Location of the mechanical holes

  The mechanical fixation of the verification PCB shall be representative of the flight configuration.
- Schematic of the mechanical stiffener if any.
- Number of PCB used for the verification programme.
- In case of verification of grid arrays device the technology used for the manufacturing of the pads and internal connections shall be the same than the FM

- For grid array devices the type of laminate used for the verification boards shall be the same than for the FM.

3. Material used

- Solder paste designation and composition (to be compliant to the ECSS-Q-ST-70-08C or 38C)
- Solder wire composition with its associated flux (to be compliant to the ECSS-Q-ST-70-08C or 38C)
- Flux used (for pretinning and soldering). Designation of flux class (ROL0, ROL1...) shall be identified.
- Conformal coating
- Adhesive (for mechanical, for thermal, for grounding...)

If these information are available in the PID compliance to the PID shall be made.

- Solvent
- Any others

4. List of components

The information shall be provided as follow

Component	Package	manufacturer	Assembly method	Bonding	Terminal material	Lead finish	Degold/pretin	Number of devices	Number of repair
Chip ceramic capacitor	C0805 type 2	XXX	VP			Sn/Pb	N/A	3	
Chip ceramic capacitor	C0805 type 2	YYY	HS			Sn/Pb	N/A	3	1 part of the 3
IC	CQFP 352 top brazed. Pitch: Lead thickness:	ZZZ	HS	In the corner using EC2216	Kovar	gold	Yes	3	1 part out of the 3 assembled
IC	FP16 Bottom brazed	VVV	HS		Alloy 42	gold	yes	3	1 part out of the 3 assembled

Note 1: A dedicated assembly form is recommended where all information which concern preparation of the device, assembly method and bonding are available.
Note 2: It is under the responsibility of the company to ensure that the soldering method and temperature is compliant with the manufacturer datasheet and or technical notes.
Note 3: The devices assembled by machine reflow shall not be reworked. Reworking will be decided during the MIP1.

- When the purpose of the verification is to verify the assembly by machine, 3 devices assembled by machine shall be mounted and 3 devices assembled by hand shall be mounted on the PCB. 1 of the hand soldering device shall be removed and replaced by hand to demonstrate the ability of the company to perform a repair.
- When the purpose of the assembly is to verify the assembly by hand only, 3 devices assembled by hand shall be mounted on the PCB exception made for the critical devices listed in the document TEC-QT/2012/206/CV (enclosed). One of the hand soldering device shall be removed and replaced by hand to demonstrate the ability of the company to perform a repair.
- Exception to the number of devices shall be considered for critical devices (See TEC-QT/2012/206/CV). In this case a minimum of 5 devices instead of 3 shall be assembled.

  The actual considered critical devices are the following:
  - Ceramic chip resistors: R1206, R2010, R2512 due to extensive cracks in the solder
  - LCCs package: All packages due to extensive cracks in the solder
  - JLCC4 (currently package of oscillators) due to extensive cracks in the solder
  - SMDs package : SMD0.5, SMD5C, SMD1, SMD2 due to crack in the ceramic package
  - Ceramic chip capacitors for which the failure is identified in the ceramic as a crack. The crack is not visible from the outside during visual inspection.
  - CWR06 packages: Cracks in the silver loaded epoxy.

- The number of devices to be assembled in case electrical monitoring is considered as a pass/fail criteria shall be as a minimum of 32 devices (with exception to grid array devices).
- A minimum of 3 devices to be verification tested by electrical monitoring shall be miscrosectioned at T0 in order to ensure compliance of the assembly (reproducibility of stand-off if applicable, acceptable wetting, absence of damage of the component, PCB, ...)
- As a minimum one failed device shall be microsectioned to identify the failure mechanism.

Note: The electrical monitoring parameters and procedure will be defined case by case as this technic is a novel procedure.

When the device is bonded underneath demonstration of the removal after bonding shall be made. In this case it is recommended to have the repair configuration used for this purpose.

5. Environmental test conditions

- Compliance of the environmental conditions of the mission (including ground testing) with the ECSS-Q-ST-70-38C, in order to ensure that the tests requested in the ECSS are sufficient to cover the application. The analysis shall identify if the mission has condition that are generally not envelopped by the test defined in the ECSS-ST-Q-70-38C as: long storage, extensive ground testing, mechanical stress after launch, high temperature application with or without thermal cycles. Compliance to the -55C/+85C for mission shall be clearly stated.
- The levels and duration of the vibration shall be identified. Statement such as compliance with the ECSS-Q-ST-70-38C will not be considered acceptable as different levels exist. It is the responsibility of the contractor to ensure that the levels applied are sufficient to cover the mission.
- The mounting configuration for the vibration tests shall be identified. The PCB shall be mounted in a way representative of the mounting of the flight hardware. Hard mounting with the PCB being in direct contact with the vibration plate shall not be considered acceptable.
- As per the ECSS-Q-ST-70-38C the accelerometers shall be placed on the PCB as well as on the base plate in order to evaluation the acceleration as well as the deformation of the PCB.
- The thermal cycling between -55/+100C is only valid when the thermal analysis for the mission shows that the electronic hardware will be working (functional and not functional) between -55C and +85C.
- In case electrical monitor is used (grid array devices) acceptance failure criteria based on the most demanding use shall be defined by the contractor.
- Shock tests shall be added when assembly of Area Array devices is part of the verification programme

6. Microsections

The microsections shall be performed at the completion of the environmental test and in compliance with the TEC-QT/2010/38/CV (enclosed document).

1. The company which will perform the microsections shall be identified in the verification programme.
2. Microsection shall be performed in the companies , laboratories approved by ESA . A list of laboratories recommended by ESA is provided in Annex 3.
3. When in house microsection facilities exist, the company shall demonstrate its capability on a representative sample (chips, LCCs, FP) having been conformally coated. In addition the understanding of the ECSS shall be

demonstrated. A report with associated microsections shall be sent to ESA for review and assessment of quality of microsectioning

4. Other laboratories. The company shall ensure when conditions 2) and 3) are not met that the quality of microsectioning is acceptable as well as that the ECSS requirements are understood. A report with associated microsections shall be sent to ESA for review and assessment of quality of microsectioning At least one device per type and size shall be microsectioned. Devices being assembled in different configurations such as machine reflow, hand soldering, hot air assembled, different bonding configurations,... shall be microsectioned.
5. All critical devices whatever their assembly configuration shall be microsectioned.

7. Pass-fail criteria parameters

   In addition to the ECSS-Q-ST-70-38 any cracks in the adhesive, lifting of the adhesive, damage to the component, damage to the printed circuit board shall be considered as a failure.

   Note: It is recommended to have an intermediate visual inspection during thermal cycling in order to assess when crack, lifting in adhesive appears.

8. Manufacturing work flow

In order to ensure full support from the Agency the progress of the verification programme shall be known. In order to ensure this the following steps shall be added in the verification programme.

1. Verification Review (VR) during which the verification programme will be reviewed and Approved by ESA. The verification programme can be signed by the Agency if deemed necessary by the company.
2. Design Review (DR) of the PCB. Information of the Paragraph 2 will be needed to conclude successfully the review. A successful DR will be concluded by the authorization to procure the PCB.
3. PID status review
4. Audit of the manufacturing line
5. Manufacturing Readiness Review (MRR). During the review the Agency will check that the verification programme has been approved by all parties and that all open actions have been closed.
6. Mandatory Inspection Point (MIP 1) before conformal coating. ESA shall be invited to the MIP1.
7. Test Readiness Review (TRR) during which the MIP records shall be reviewed. The Verification programme shall be at this stage approved and signed by all parties. The vibration, shocks and thermal procedures shall be provided and reviewed during this review.
8. Mandatory Inspection Point (MIP2) at the completion of the environmental test. The Agency shall be invited to the MIP2.
9. Test review board (TRB) during which the environmental tests results will be reviewed. All open NCRs (minor and major) shall be reviewed and closed.

10. Final verification review during which the microsections reports, electrical monitoring results will be reviewed. The Assembly processes will be reviewed during the meeting in order to have the PID issued. Verification of closure of the actions identified during the audit of the manufacturing line. It is the objective of the review to agree on the content of the Summary Tables.
11. Approval of Summary table and final approval of PID and related procedures

9. NCRs

Any NCRs related to the assembly shall be reported to the Agency. If needed NRBs shall be organised by the contractor.
It is the intention of the Agency to organise a ftp server such as NCTS where the NCRs will be uploaded. Contractor will be informed when the ftp server will be on service.

10. Verification by similarity

- Verification by similarity shall be applied in compliance with the ECSS-Q-ST-70-38C.
- It is advised for critical devices to add intermediate size in case the biggest device fails.
- Verification by similarity does not apply for LCCs package.

11. Certification status of the operators and inspectors

The compliance with the ECSS-Q-ST-70-08C shall be identified.

12. Compliance of the manufacturing room

The compliance with the ECSS-Q-ST-70-08C shall be identified.

Annex 2

Additional information needed related to the verification programme

1. Planning

The detailed chart shall be provided.
Update of the planning will be provided during the different step identified in Paragraph 7.

2. Vibration test procedure

The content of the vibration test procedure shall be as followed:

1. List of Applicable documents
    a. Project Requirement
    b. ECSS-Q-ST-70-08C
2. Company selected to perform the vibration
3. Test set up
4. List of the PCBs to be tested with their associated layout
5. Schematic of the PCB mounted with its frame (to ensure that the stiffener is sufficient for the vibration levels)
6. Schematic of the test adapter
7. List of the test instrumentation
8. Location of the accelerometers
9. Test conditions (Temperature, Pressure, Humidity, cleanliness) and tolerances (Frequency, Amplitude, sweep rate, power spectral density, random overall, test duration)
10. EMC conditions when applicable
11. Tests levels
    a. Resonance search
    b. Sine vibration
    c. Random vibration
12. Test flow
13. Success criteria

3. Thermal cycling test procedure

The content of the vibration test procedure shall be as followed:

1. List of Applicable documents
    a. Project Requirement
    b. ECSS-Q-ST-70-08C
2. Company selected to perform the thermal cycles

3. Test set up (thermo couple mounted on the boards)
4. List of the PCBs to be tested
5. Mounting configuration of the PCB in the thermal chamber
6. List of the test instrumentation
7. Test conditions (Temperature, Pressure, Humidity, cleanliness, slopes, dwell time, number of cycles, atmosphere of the thermal chamber) and temperature tolerances
8. EMC conditions when applicable
9. Test flow

ANNEX 3

List of ESA PA Managers with its associated programme (List subjected to change in the future)

Last name	First name	Position	Projects
Damiano	Giovanni	Product Assurance Manager	Expert
Ferrer	Sonia	Product Assurance Manager	ERA /ATV
Kaspers	Martin	Product Assurance Manager	EGNOS
Admiraal	Willem J.	Ground Segment Product Assurance Engineer	Galileo
Aldea Montero	Fernando	Galileo Software PA Manager	Galileo
Azcarate Lupiola	Jose	Msg Product Assurance Manager	MSG-Metop 3
Monteiro	David	Product Assurance Manager	Gaia
Beurtey	Xavier	Product Assurance Manager	Ariane
Brown	Andrew	Galileo Ground Segment PA Manager	Galileo
Pierre	Brunner	Product Assurance Manager	IXV
Bussu	Giancarlo	Product Assurance and Safety Manager	ISS Utilisation
Di Cosimo	Gianluigi	Hd of the GMES Space Segment PA & S Office	Sentinel 2
Chase	Richard	Product Assurance & Safety Manager	ATV Operations
Chevrier	Muriel	Quality Engineer	D/OPS Quality Office
Hall	John	Product Assurance Manager	Galileo
Di Mascio	Simone	Software Product Assurance Engineer	Galileo
Falcolini	Massimo	Product Assurance Manager	JWST
Flamand	Jean-Francois	Product Assurance Manager	Sentinel 3
Fogli	Carla	Galileo Satellite Product Assurance Manager	Galileo
Frigo	Alexander	Quality Engineer	D/OPS Quality Office
Garat	Francois	Product Assurance & Safety Manager	@sat
Geary Norrenbrock	James Hermann	Product Assurance & Safety Engineer	MTG
Verna	Marco	PA Engineer	Vega
Garat	Francois	Product Assurance Manager	EDSR
Herd	Andrew	Operations Safety Manager	Operations
Hopkins	John	Product Assurance Manager	Small GEO Platform Programme
Huesler	Joseph	Product Assurance & Safety Manager	LISA Pathfinder
Kasper	Michael	Product Assurance Manager	Exomars
Lefort	Eric	H/ Launchers Prod Assur and Safety Office	Ariane
Linner	Herbert	PA Engineer	Vega
Lock	Tim	Product Assurance and Safety Manager	ESAC
Mantineo	Alfio Roberto Maria	Head of D/OPS Quality Office	D/OPS Quality Office

Marcos Sbarbaro	Patricia	Satellite Product Assurance Engineer	Galileo
Last name	**First name**	**Position**	**Projects**
Meehan	John	Product Assur.&Materials Eng	ISS Utilisation
Norrenbrock	Hermann	Product Assurance & Safety Manager	MTG
Olivier	Pierre	Product Assurance & Safety Manager	Solar Orbiter
Panicucci	Massimo	Product Assurance Manager	Vega
Panin	Fabio	Product Assurance Manager	Bepi Colombo
Pinel	Jacques	Product Assurance & Safety Manager	Exomars
Prezelus	Sylvain	Product Assurance Manager	Swarm
Rautakoski	Jan	Product Assurance Engineer	PROBA 3, -V
Rouvier	Emmanuel	Product Assurance Manager	Bepi Colombo
Scaglioni	Stefano	PA & Safety Manager	D/OPS Quality Office
Secchi	Patrizia	Product Assurance Manager	Sentinel 1
Simonini	Andrea	Quality Assurance Manager	PDS / EOP Apps
Soulez Lariviere	Cyril	Product Assurance Engineer	Sentinel 5
Spence	David James	Product Assurance Manager	EARTHCARE
Torres Tomas	Eloy	Senior Product Assurance Engineer	Large Platform Programme
Vicari	Emmanuel	Product Assurance Engineer	D/OPS Quality Office
Villar Ruibal	Paloma	Product Assurance Manager	Seosat
Vivar y Cerrato	Maria de la Asuncion	Software Product Assur.Eng.	Galileo
Watts	Nigel Ronald	Head of Product Assurance & Safety Office	Galileo
Wernham	Denny	Product Assurance Manager	Aeolus
Woop	Gregor	Head of the ISS PA&S Coordination Office	ISS Programme

ANNEX 4

List of companies recommended to perform microsections (List subjected to change in the future)

- Hytek in Denmark
Mister Poul Juul
Sofievej 61
DK- 9000 Aalborg
Denmark
Phone: +4598117003
e-mail: hytek@hytekaalborg.dk

- IIS in Italy
Mister Luca Moliterni
Lungobisano Istria 15A
I-16141 Genova
Italy
Phone: +34(010)8341315
e-mail: luca.moliterni@iis.it

- Serma technologies in France
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e-mail: m.leveque@serma.com
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- ZVE in Germany
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MEMO

Date	14 January 2013	**Ref**	TEC-QT/2012/206/CV
From	Carole Villette	**Visa**	T. Ghidini
To	Companies having ESA Approved Summary Tables or under verification programme	**Copy**	PA Managers

Subject: Identified critical devices for the assembly as per ECSS-Q-ST-70-38 on PCB laminates

During the past years some failures on solder joints or in devices have been identified at the completion of the environmental testing performed in compliance with the ECSS-Q-ST-70-38C.

It is the intention of ESA to inform industry, when not already done in order to prevent the use of these devices or to identify possible corrective actions.

The list of devices is not exhaustive and some devices may be missing. In the future, this list will be updated every time new failures are documented.
The criticality has been identified when the failures in the solder joints and/or in the devices have been noticed in many occasions by different end users.
In many cases it has also be concluded that failures could occur to a process not compliant to the component manufacturer assembly recommendations. In these cases the component was not considered as critical. In general, these failures have been identified thanks to the improvement of the quality of the microsections requested by ESA in the last years as well as increase of number of microsectioned devices and terminals.

Some of the failures identified in the table may result to the large temperature range used during the thermal cycles and may not appear when the temperature range is reduced. Reduction of temperature range will result in an increase of number of cycles.

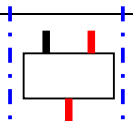
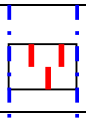
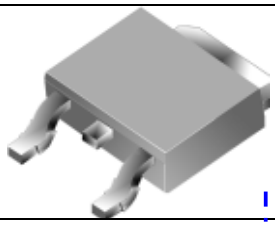
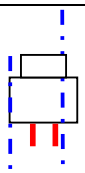
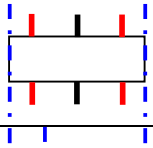
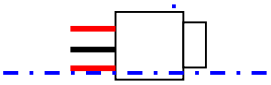
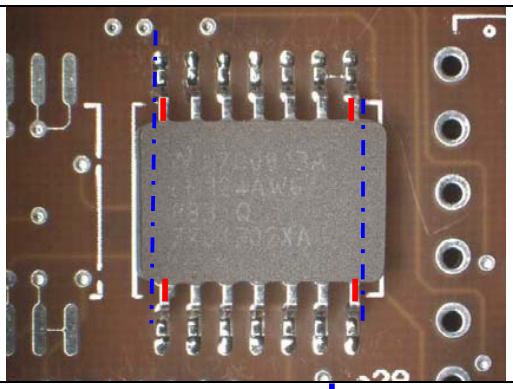
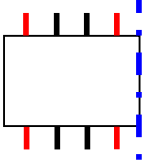
In addition to the failures listed in Table 1, a failure due to excessive conformal coating has also been identified.
It is recommended that conformal coating is used such that it does not negate the stress relief and does not fully encapsulate the devices. Indeed during thermal cycling the conformal coating is responsible to additional stress and may lead at some extend to cracks in the solder joints.
Once verification test in compliance with the ECSS-Q-ST-70-38C have been completed and are considered successful, the amount of conformal coating shall not be modified since otherwise the ESA Approval status will no more be valid.

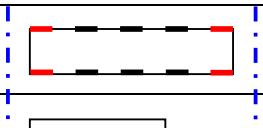
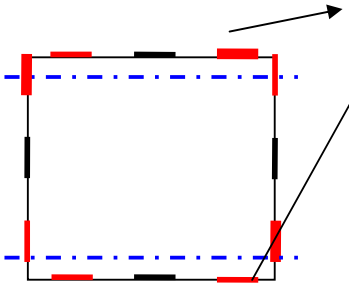
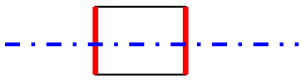
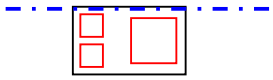
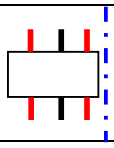
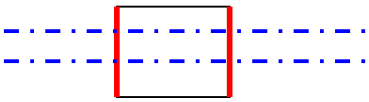
Component	Package type	Type of failure	Recommendations and or notes
Chip Resistor	R1206, R2010, R2512	Cracks in the solder joint	- To increase the stand off. Such corrective action may not be sufficient.
Chip Capacitors	Any	Crack in the ceramic initiated at the end termination	- To follow component manufacturer recommendations (preheating of the board, device and limited temperature) - Rework of such capacitors shall not be performed. In case of rework needed replacement of the device is recommended.
	LCCs	Crack in the solder joint	-Degolding and preheating temperature used to be compliant to component manufacturer datasheet - To increase the stand off -To solder the device upside down and add gull wing terminations (need of verification in compliance with ECSS). Change of solder footprint is required. - To solder upside down and have long wiring implemented. - Not to consider any verification by similarity for such package.
Tantalum capacitors	CWR06	Crack in the device. Crack in the epoxy between the tantalum and the terminal.	- Use of TAJ/ CWR packages for which the temperature is not directly spread to the package.
	SMDs (SMD0.5, SMD1, SMD2, SMD5C)	Crack in the ceramic	-Procurement of package with terminations when possible which require a change of design of the solder footprint. - Assembly upside down using thermal adhesive and addition of wires or ribbons. This configuration may not be adapted for high thermal dissipation need.
Oscillator	JLCC4 with bottom brazed terminals	Crack in the solder joint	- Failure due to stiffness of the terminals combined with missing stress relief.
Stacked devices	SOP from 3D+	-Crack in the solder	-Procurement of devices with

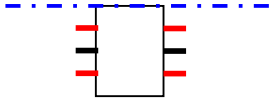
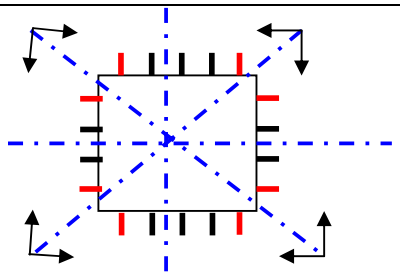
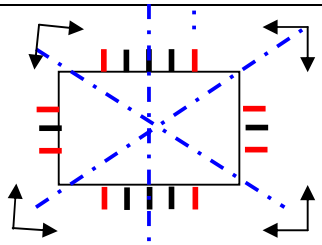
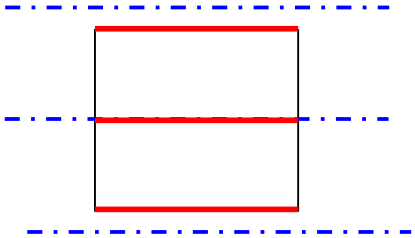
		joint -Unacceptable per ECSS-Q-ST-70-38C solder height at heel when hand soldering -No possible visual inspection possible due to the shape of the terminals -Restrictive soldering temperature (reflow and Hand soldering)	shortened leads (around 3 mm instead of 5 mm)
Stacked capacitors	CNCXX	- poor wetting due to finish type 10 (Ag 98%) -poor co-planarity of the leads	- To pre-tin the device
Photo transistor	Pill from micropac	- Cracks in the solder joint of the two small terminals	- To degold and pretin at temperature compliant to the component manufacturer recommendations. - Not to solder the bottom part on the PCB but to make a wiring connection.
inductor	Coilcraft inductor AE235 type	Poor wetting of the terminals	-To request coilcraft for additional cleaning of the terminal to remove the contamination from the enamel present on the terminal.
	Enamel wire	Short due to damaged enamel	-Recommendation to add an insulation (kapton, brady label, filled varnish...) to avoid contact with metallic traces..

Table 1: List of identified critical devices for the assembly as per ECSS-Q-ST-70-38 on PCB laminates.

Microsection guidelines:

SOT23:	
LCC3	
TO252	 
SO20	
LCC6	
D2 Pack	
FP	
SESI	
Chip resistor	

MM series resistors	
CRA 12E and array resistors	
CTC	
LCC with terminations on 4 faces	 To check during microsection of other pins
MPCI	
DO213	
D5-B	
SMD	 To check ceramic cracks
SOT223	
PM94-S4	 Only one termination for the new devices
CWR	

CH51	
CQFP To cut after embedding	
MQFP	
Area Array devices	

To check absence of damage of the PCB

Location of the microsection
Leads to be microsectioned