meeting date *date de la réunion*	26 of May 2009	ref./*réf.*	TEC-QT/2009/1059/CV	page/*page*	1 3
meeting place *lieu de la réunion*	ESTEC	chairman *président*	C. Villette (TEC/QTM)		
minute's date *dates de compte rendu de réunion*	14/09/2009	participants *participants*	F.P. Gracia (Crisa), L. Douguet (Astrium Velizy), N. Wazad (Astrium Velizy), S. Dackham (Astrium Portsmouth), N. Venet (TAS Toulouse), J.P. Bessaguet (TAS Toulouse), Th. Battault (CNES), P. Allard (Ruag Sweden), S. Mattson (RUAG Sweden), S. Wallin (SSC), L. Granholm (SSC), G. Corocher (TEC-QTM), A. de Rooij (TEC-QTM), B.D. Dunn (TEC/Q),		
subject/*objet*	Request for change of verification procedure and acceptance criteria of area array package of the ECSS-Q-70-38	copy/*copie*	R. Cirone, L. Marchand, L. Balestra, Ch. Ferre (Atmel), M. Nikulainen, J. Bosma		

description/*description*	action/*action*	due date/*date butoir*
A1: Industry to provide the criteria proposed for the electrical failure of the area array packaging during thermal cycling.		As possible

1. Objective of the meeting

All companies (Astrium Velizy, Austrian Aerospace, SAAB, Syderal, Spur Electron, Comdev Cambridge, Thales Toulouse…) having performed a verification programme compliant to the ECSS-Q-ST-70-38 have failed. It indeed appears that the size of the cracks in the column after cumulated vibration and thermal cycling is exceeding the maximum allowed by the ECSS-Q-ST-70-38. Moreover it appears that in the past companies having performed a continuous electrical monitoring of the assembled package until electrical failure did show the first failure around 2000 cycles. This is why TEC/QTM has proposed a change of verification pass fail criteria for the area array packaging by organising the meeting. It was decided to present the new proposal to all WG members of the ECSS-Q-ST-70-38. In order to get feedback from company having experience with such packaging it was decided to invite also EADS Astrium Portsmouth as well as the Swedish space agency.

2. Presentation of the different companies and from Estec regarding the assembly of MCGA and CCGA (see Annex 1).

The presentations have been distributed via USB at the end of the meeting.

3. New proposal for the verification of the assembly of the area array packages

All participants have agreed on the following pass fail criteria.
The procedure to achieve the Approval of the assembly of area array device is the following:

a. Manufacture of capability samples

One device shall be assembled by machine reflow
One device shall be assembled by machine reflow – remove and replaced
In total 3 devices are needed for to manufacture the capability sample.
X-Ray and visual inspection shall be performed to ensure the compliance with table 9 of the ECSS-Q-ST-70-38C.
These two configurations shall then be submitted to vibration and 500 thermal cycles from -55/+100 degre C.
At the completion of the environmental testing microsection shall be performed to ensure that the PCB has not been damaged.
Defect such as pad lifting, cracks in laminate, cracks in via, cracks of tracks, PCB delamination… shall conclude to the reject of the assembly.
In such case the company shall not start the verification programme prior to demonstrate corrective actions.
The capability samples shall then be remanufactured and re tested.
Once the capability sample has shown acceptable results the verification programme can start.
It is possible also to determine the failure mechanism of the device during the microsectioning. This information is considered as informative.

In case the company assemble and repair using the same soldering station the assembly by machine reflow may be omitted as then the repair configuration will provide sufficient results.

b. Verification programme

Three devices shall be assembled as nominal and one device shall be assemble-remove and replaced by a new one in order to verify the repair of the assembly.
In total a minimum of 5 devices are needed.
These 4 samples shall then be submitted to vibration testing and to thermal cycling. The thermal cycling shall be performed until electrical failure.
The pass criteria shall be no electrical failure before 1500 thermal cycling.
A1: It has been agreed during the meeting that the end users shall provide us their criteria for electrical failure: Is this an open circuit or an increase of resistivity. It could be possible to provide a generic fail criterion which could be for example open circuit. In case the application requires a loss in resistivity of less than X% then the fail criteria would be such criteria. This of course could depend on application, design…

In case of electrical failure before 1500 thermal cycling then a failure investigation shall be performed.

The assembly/repair shall be performed on representative configuration (conformal coating, underfill, mechanical support…). The pcb shall be made with the same materials and the routing of the device shall be identical to the FM. Indeed the capability sample is made to ensure that the PCB is not degraded by the assembly/repair and in addition that the environmental tests do not create damage of the PCB.

In order to conclude on the verification programme it is required:

-The Daisy chain device is representative of the FM. As already agreed with Atmel the daisy chain shall be submitted to all tests made on the FM .

-The daisy chain shall be reliable. Astrium has reported during the meeting that some electrical failure was induced by cracking in the wire bonding due to the lack of stress relief.

If a verification programme has already been performed on a device with a different pitch the capability sample may be omitted with the agreement with the Approval Authority.

4. Conclusion

As soon as the electrical pass fail criteria will be determine a request for change of the ECSS-Q-ST-70-38C will be made by Estec TEC-QTM.