Metallurgical Evaluation of Steam Aged LCCC Devices following Solderability Testing

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ABSTRACT — Solderability testing, according to Military Standard 883, has evolved through four sets of different test conditions during the past ten years. These relate to the duration of artificial steam ageing and the utilisation of either mildly activated or pure rosin flux. The European Space Agency (ESA) has experienced few solderability problems with leadless ceramic chip carriers (LCCCs) supporting tin-lead finished castellations. However, similar packages having gold on nickel plated finishes will only produce satisfactory solderability results when activated flux is applied to samples exposed to steam ageing for eight hours.

A reason for poor solderability is given, based on an evaluation of test samples and metallography. It is concluded that tin-lead finished devices should be subjected to eight hours of steam ageing followed by solderability testing with pure rosin flux.

An ESA prerequisite for soldering is that all gold finishes must be removed, possibly with the aid of RA type fluxes. For this reason it is recommended that RA flux is permitted (when necessary) during the standard solderability test.

INTRODUCTION

HCMOS devices, packaged within leadless ceramic chip carriers (LCCCs), have been submitted to solderability testing as part of a general ESA qualification.[1,2] The solderability test follows a Military Standard method that has evolved since 1983, as illustrated in Table 1. Two major changes to the test were introduced in May 1987 (issue 5), these being the requirement to increase the steam ageing time from one to eight hours, and the prohibition of mildly activated (RMA) soldering flux in favour of non-activated R-type flux. Neither issue 5 nor issue 6 differentiates between leaded and leadless devices. The latest update to the Mil Std is issue 7, dated November 1991, and the solderability prerequisite is as per issues 5 and 6 that both leaded and leadless packages shall be steam aged for eight hours. Also, again the flux utilised shall be type 'R'. However, a new line has been added to issue 7: 'The customer/equipment manufacturer may, at their option, use 'RMA' flux'.

Frequent changes to component package solderability test requirements, as reflected in Table 1, have caused some confusion to ESA package qualification programmes and to the solderability tests made either at incoming inspection or just prior to solder assembly by ESA contractors. An omission to notice the permitted issue 7 option for using 'RMA' flux has meant that test programme plans and company in-house quality procedures have not been updated and 'R'-type fluxes continue to be employed. An evaluation of the effectiveness of 'R' flux during solderability testing has been made in order to better understand low yields at the onset of package qualification programmes.

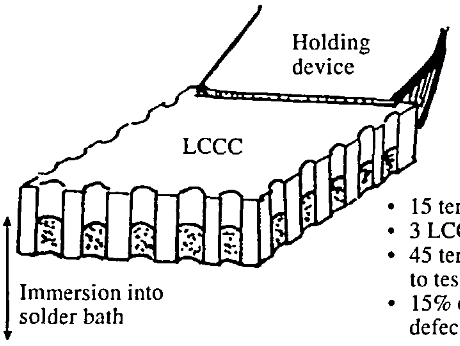
Solderability test results have shown that, whereas the castellations of LCCCs having tin-lead terminations will regularly pass the requirements for at least 95% coverage by a continuous new solder coating, those possessing a gold finish are prone to fail the test. This paper considers the reasons why gold terminations fail the Mil Std solderability test if non-activated flux is prescribed following steam ageing.

THE SOLDERABILITY TEST METHOD[2]

The LCCCs are steam aged for eight hours. They are placed on a ceramic support plate which is held between 1.5 and 3.0 inches above boiling deionised water. There is no precleaning of the packages or their termination areas. Following steam ageing the packages are air dried for 2 hours, immersed in R flux for 5-10 seconds then solder dipped at 245± 5°C for 5± *0.5 seconds. The angle of immersion is between 30 and 45°* from normal (for each edge). After solderability testing they are rinsed clean in isopropyl alcohol and each termination area is then inspected at 20 times magnification. These packages have 20 terminations and are generally tested in groups of three.

As shown in Figure 1, a total of 38 terminations are inspected (the lot allowed percentage of defects being 15%). Although two solder dipping operations are permitted, this has not been found to increase the yield of passes. The criteria for acceptable solderability during the evaluation of the terminations are:

(i) The total surface area of the dipped castellation termination and pad is at least 95% covered by a continuous new solder coating.
(ii) Pinholes, voids, porosity, non-wetting or dewetting are not concentrated in one area and do not exceed 5% of the total area.



- 15 terminations
- 3 LCCCs per lot
- 45 terminations exposed to test
- 15% of which may be defective due to test operation (difficulty in holding these small devices)

∴ 38 given full inspection

Fig. 1 *Account of castellations inspected — the 15% defective are adjacent to the holding device.*

SOLDERABILITY TEST RESULTS

The initial qualification test programme involved the testing of three LCCC devices and resulted in 27 termination areas out of the 38 inspected showing less than 95% solder coverage. This result is designated: 27 FAILS/38.

Table 1

Mil Std-883 Method 2003 Historical Differences

Method 2003-3	Method 2003-4	Method 2003-5	Method 2003-6	Method 2003-7
(Aug. '83)	(Nov. '85)	(May '87)	(Mar. '89)	(Nov. '91)
All packages	Leaded packages	All packages	All packages	All packages
— Flux: Type R or RMA	— Flux: Type R	— Flux: Type R	— Flux: Type R	— Flux: Type R (RMA optional)
— Ageing: 1 hour	— Ageing: 4-8 hours	— Ageing: 4-8 hours	— Ageing: 4-8 hours	— Ageing: 8 hours
	Leadless chip carriers			
	— Flux: R or RMA			
	— Ageing: 1 hour			

Table 2

Previous Solderability Test Results* for LCCCs and Side Brazed Packages using Different Flux Activities and Various Temperatures

	Without Steam Ageing						*With 1 Hour Steam Ageing (i.e., issue 3 ageing requirements)*						
Solder Bath Temperature	240°C		250°C		260°C		Solder Bath Temperature	240°C		250°C		260°C	
Flux	R	RMA	R	RMA	R	RMA	Flux	R	RMA	R	RMA	R	RMA
Chip Carrier	0/10	0/10	0/10	0/10	0/10	0/10	Chip Carrier	-	-	10/10	0/10	3/10	0/10
Side Brazed	0/10	0/10	0/10	0/10	0/10	0/10	Side Brazed	1/10	0/10	0/10	0/10	-	-

* Acceptance criteria: Mil Std-883 — Method 2003 Number of failed devices/number tested.

The manufacturer undertaking this programme stated that earlier test programmes had employed issue 3 of the test method (see Table 1). This had provided satisfactory results and the increase in ageing time from one hour to eight hours constituted an unacceptably harsh simulation of accelerated ageing. The previous test results are shown in Table 2.

In order to evaluate the effectiveness of different flux types and to simulate actual de-golding and pre-tinning processes a further series of solderability tests were undertaken at two different manufacturing sites. The results of these recent tests are shown in Tables 3 to 5.

Table 3

LCCC Solderability Test Results (per Mil Std-883-Method 2003 Issue 6 at Site A)

Test	*Devices Tested*	*Steam Ageing*	*Flux*	*Result**
A	3	8 h	RMA (Alpha 615-25)	4/38
B	3	8 h	RA (Kester 1429)	0/38
C	1	1 h	R (Colophony)	0/20
D	3	1 h	RMA (Alpha 615-25)	0/38

* (Terminations failed/total inspected)

Table 4

Further Tests at Site A

Test	*Devices Tested*	*Steam Ageing*	*Flux*	*Result**
A	3	8 h	RMA (Alpha 615-25)	25/38
B	3	8 h	RA (Kester 1429)	0/38
C	3	8 h	RMA (Alpha 615-25)	8/38
D	3	8 h	RA (Kester 1429)	0/38

* (Terminations failed/total inspected)

Table 5

LCCC Solderability Test Results at Site B

Test	*Devices Tested*	*Steam Ageing*	*Flux*	*Result**
A	20	8 h	RMA	20/20
B	20	8 h	RA	0/20
C	15	1 h	R	7/15
D	10	1 h	RMA	0/10

* (Devices failed/total inspected, each device supported 20 terminations)

METALLURGICAL EVALUATION

Visual inspection of the solderability test samples showed clearly a wide range of results, ranging from excellent wetting of solder onto both the gold-plated base and castellation of each terminal, to poor wetting and occasionally only 75% coverage (filling) of some castellations. When Tables 2 to 5 are analysed, it is clear that the application of pure rosin flux (colophony) will provide suitable solderability of as-received devices, questionable solderability of devices steam aged for one hour and total failure to pass the test after eight hours of steam ageing.

Two devices were submitted to metallographic evaluation. One was in the as-received condition; the other was taken from the initial qualification test programme which had resulted in 27 FAILS/38 (i.e., a device that had been steam aged for eight hours and tested with pure rosin flux, then cleaned in isopropyl alcohol). The undersides of the two samples were photographed (Figure 2). The photographs of the castellations in Figure 3 show the initial roughness of the alumina package side faces. The

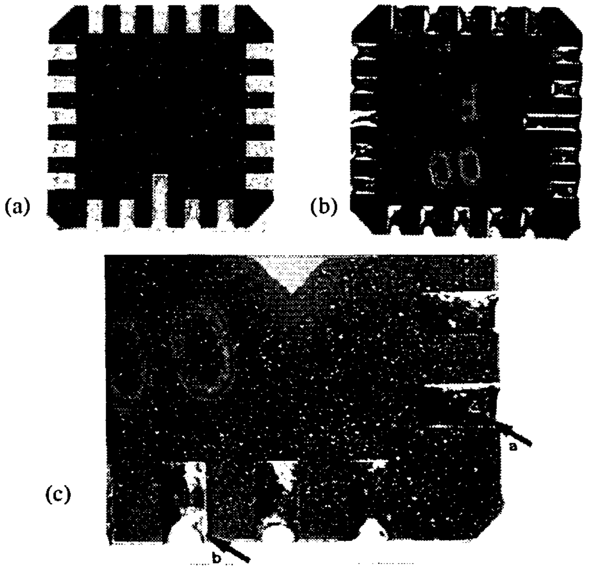


Fig. 2 *Optical photographs showing the bottom side of leadless ceramic chip carrier packages before and after the solderability test (steam ageing then solder dip utilising non-activated rosin flux 'R'). (a) As received. (x 3) (b) Following steam ageing and solderability test. (x 3) (c) Detail of (b) showing along side 'a' good flow of solder into castellations but some localised non-wetting of pad. Side 'b' shows poor flow into castellations and larger non-wetting areas on pad. (x 12).*

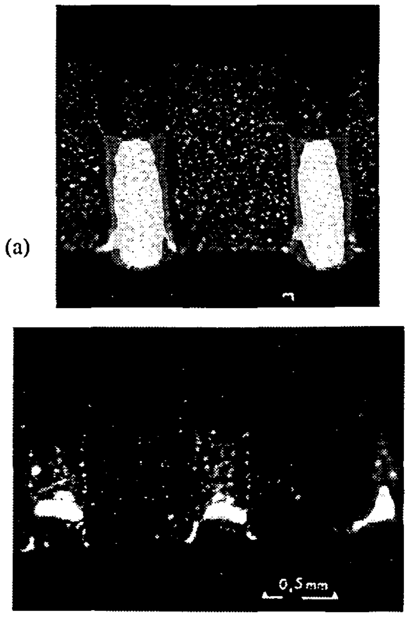


Fig. 3 *Photographs before and after solderability testing. (a) Gold finish. (b) Best side for solder flow. Note the rough speckled gold finish within the castellations and, after solder dip, the non-uniform solder fills.*

metallisation and plated layers within each castellation replicate this roughness and where solder wetting has been achieved it does not have a consistently bright, smooth appearance.

The devices were mounted in a low exothermic resin, then ground and polished to reveal the cross-section of as-received metallisations and platings, partially wetted base pads and partially filled castellations. The partially wetted base pad seen in Figure 2 is shown in cross-section in Figure 4. The irregular nickel layer is well attached and follows the undulations of the tungsten metallisation. The nickel layer varies in thickness from 0.8 to 2.0 microns. Importantly, it contains many peaks and re-entrants which are covered by a gold layer of between 2 and 5 microns. Small areas of non-wetted gold are surrounded by solder fronts having rather good wetting angles (from 10 to 45°). No exceptionally high wetting angles were observed and no cases of dewetting.

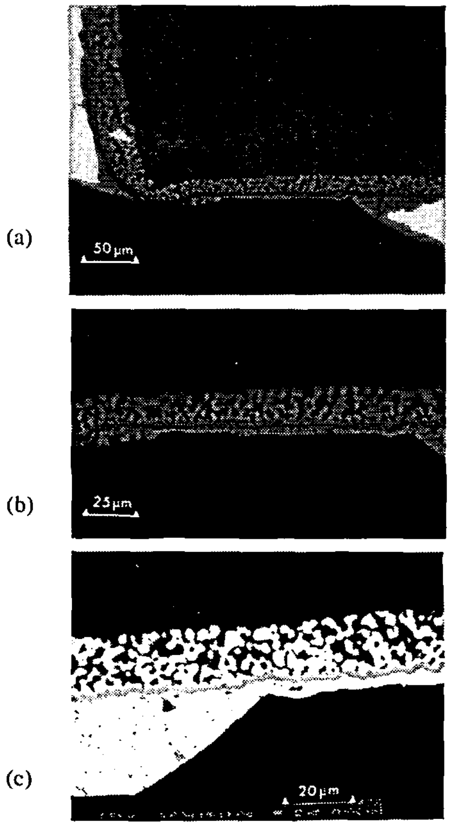


Fig. 4 *Polished microsection through the LCCC transverse direction so as to intersect the partially wetted bottom pad termination arrowed in Fig. 2 (c). Except for the rough nickel and gold layers there is nothing to account for this partially wetted pad. (a) Optical micrograph. (b) As (a), to highlight plated layers and solder wetting angles. (c) SEM backscatter view of solder fillet (reverse image of (b)).*

The microsectioned castellations also revealed relatively low wetting angles as shown in Figure 5 (following eight hours of steam ageing). Figure 5 also highlights the exceptionally rough nickel underplating and similarly rough gold finish. An attempt was made to compare the elemental distribution across as-received (non-aged) LCCCs and LCCCs that had been subject to eight hours of steam ageing and then failed the solderability test due to complete non-wetting by solder and 'R' flux. The line-scan results are detailed in Figure 6. Each layer is clearly revealed by means of back-scatter electron imaging. The outer gold finish may be dense or somewhat porous (compare Figure 6(a) with 6(b)). The oxygen line-scans are inconclusive but do indicate a more variable oxygen content within the slightly thicker and more porous aged gold plating (compare (c) with (d)). It is important to note that both tungsten and nickel appear to be present within the thicker gold plating. This effect is caused by the presence of a protruding tungsten metallisation particle, covered with nickel, and lying just beneath the cross-sectioned gold layer (compare (e) with (f) and (g) with (h)).

DISCUSSION

The processes involved in the manufacture of LCCC devices are not known in detail. The metallographic results contained in Figures 4-6 indicated that the tungsten metallisation terminations have been applied to alumina ceramic as an ink and then fired to cause sintering of the individual tungsten particles. This surface was then nickel plated either by an electroless or by an electrochemical process. The gold finish is probably applied by electrochemical plating from a cyanide bath.

It will be recognised that the LCCC terminations have a completely different form and material composition from leaded packages. The plated layers on component leads such as Kovar, 42FN alloy or other nickel alloys are generally smooth, dense and present as a 'protruding' lead. Such axial lead terminations will have a low thermal mass at the moment when immersed into liquid solder. When wetting has not quite started, there is an upward force made up of lead buoyancy and negative surface tension forces. When leads have good solderability, the solder meniscus wets and forms a low contact angle with the lead. The surface tension force becomes positive and solder will quickly flow over the surface layer, either fusing with it in the case of tin-lead finishes, or alloying with it in the case of gold finishes.

The LCCC package edges, as with most surface mounting component terminations, must be completely immersed into the solder bath in order to perform the solderability test. The surface tension forces and solder meniscus associated with a three-dimensional castellation surrounded by non-wetting ceramic surfaces will be far more complex than the conventional 'protruding' lead. Similarly, the thermal capacity of the LCCC will be far greater than that of an individual lead during solder immersion. These facts question the suitability of a solderability test which encompasses both leaded and non-leaded packages without allowing for the prediction of how well each device will solder in production.

The general ESA soldering specifications for both leaded devices[3] and leadless surface mount devices[4] require that gold shall be removed from terminations prior to solder assembly and replaced with a tin-leaded dip finish. This will avoid the formation of brittle tin-gold intermetallics which are known to severely jeopardise the reliability of solder joints.[5]

It will be remembered from the Introduction that LCCCs possessing tin-lead finishes had no problem passing the solderability test even following eight hours of steam ageing. Clearly, gold-plated terminations will only be kept in this as-received condition during storage of the devices. At some time prior to assembly they will be degolded and pretinned by standard processes which permit the use of active fluxes (even corrosive acid fluxes) to facilitate gold dissolution and proper wetting.[3,4]

Solderability testing is only performed on a limited number of samples during device incoming inspection and as part of the initial ESA qualification of a new component type or supplier.[1] The test should detect even relatively subtle soldering problems and it is for this reason that the flux used possesses a low activity, as prescribed in the Mil Standard

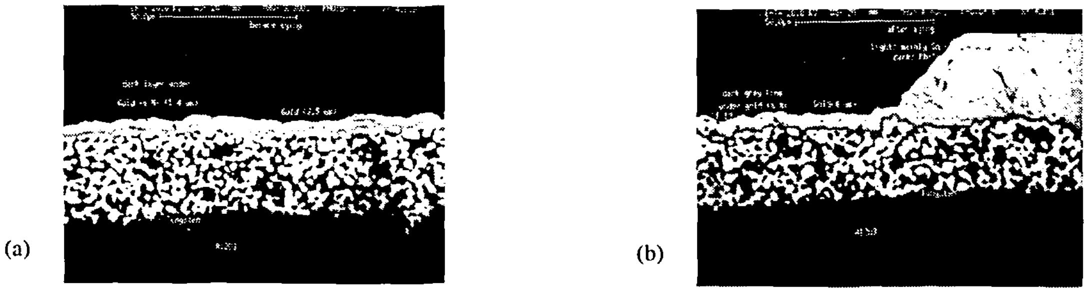
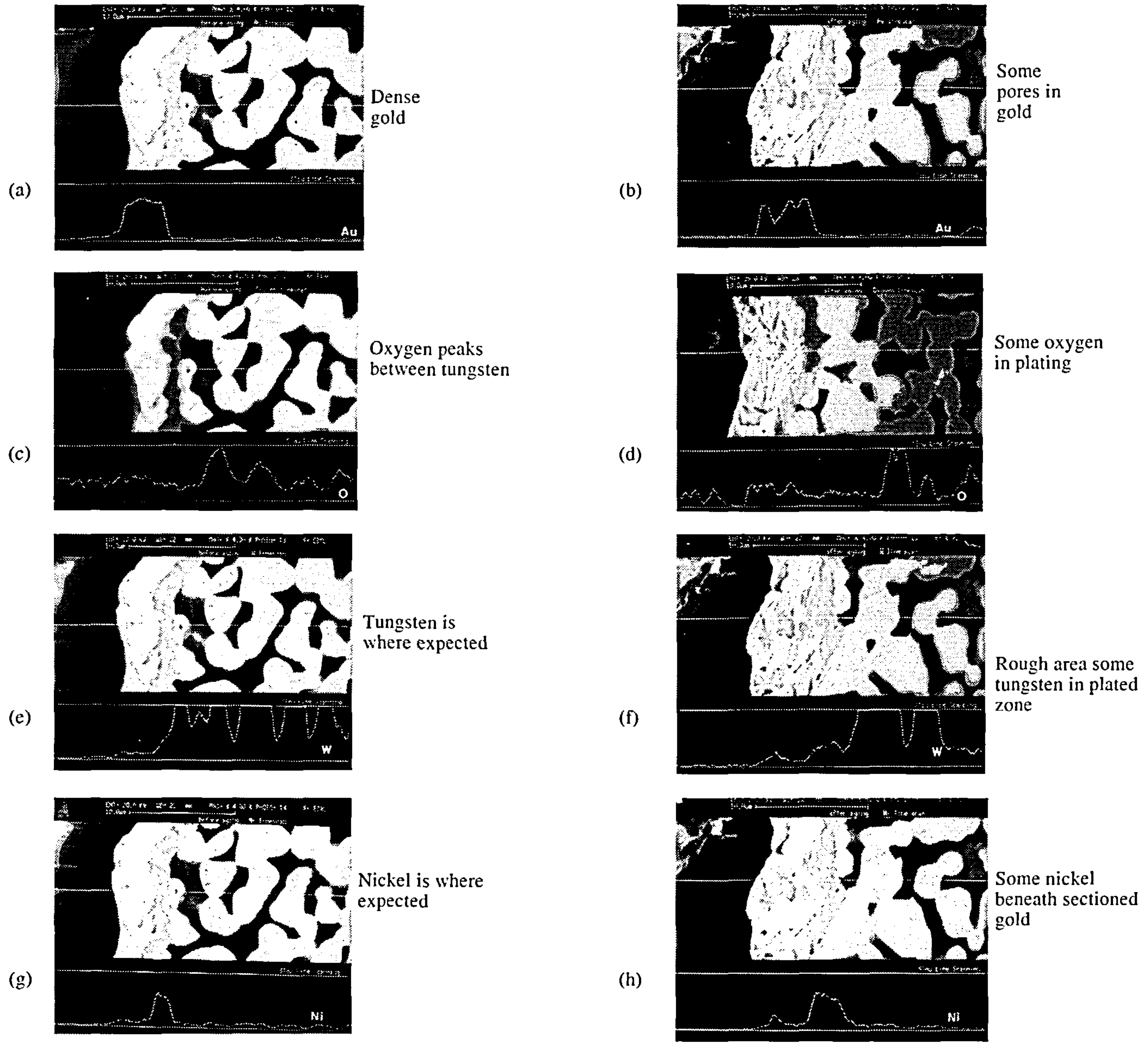


Fig. 5 *Polished microsections in the LCCC transverse direction along the metallised castellations. SEM backscatter (atomic number) micrographs to highlight the various layers. (a) As-received. (b) After solderability test — failed due to partial wetting of castellation. Note: the higher the atomic number, the brighter the image of that layer.*



Dense gold

Some pores in gold

Oxygen peaks between tungsten

Some oxygen in plating

Tungsten is where expected

Rough area some tungsten in plated zone

Nickel is where expected

Some nickel beneath sectioned gold

Fig. 6 *Line scans across metallised/plated castellations. (a), (c), (e) and (g) As-received LCCC. (b), (d), (f) and (h) After 8 hours' steam ageing (in non-wetted region).*

(type R rosin flux).[2] The test results included in this paper show that LCCC packages with gold finished castellations under ESA qualification do not pass the solderability test when type R flux is employed. It would seem that, only by applying active fluxes, classified as type RA, can solderability be guaranteed following eight hours of steam ageing. The poor performance of the metallised castellations is thought to be caused by a combination of factors:

1. The intermediate nickel plating on tungsten metallised LCCCs is very rough compared with electroplated finishes on standard leads. This roughness retards the solder wetting process as the solder meniscus dissolves and progresses over the gold surface finish.
2. Nickel peaks and porous gold enhance the diffusion of oxygen into the plated layer during steam ageing to cause oxidation of the nickel. Gold and nickel are separated by an EMF potential of 0.45 V in the electrochemical series table[5] and this will promote galvanic corrosion/oxidation of the nickel sub-surface. Only active flux can remove this internal nickel oxidation layer.
3. Terminations (castellations) on LCCC packages have a much greater thermal mass than the protruding leads on conventional packages. The greater thermal mass delays solder wetting on LCCCs by reducing the temperature of the advancing solder meniscus, reducing the fluxing and delaying the surface chemical reactions between flux and oxide films.
4. The rough surfaces of the LCCC castellations act as cavities which entrap solder flux. During solder immersion the flux volatilises, causing local cooling of the solder volume (latent heat of evaporation), and bubbles of gas, partially held by the rough surfaces, prohibit 100% solder wetting. Flux present on conventional leads reacts with surface films and is easily swept away during immersion into liquid solder.

The solder contact angles illustrated in this paper (Figures 4 and 5) show that partial wetting has occurred. Non-wetting and dewetting were not observed. The satisfactory solderability test results seen in Table 2 for LCCC castellations in the as-received (non-aged) state are in marked contrast to the subsequent tables which show a progressive worsening of solderability as artificial steam ageing exposure is increased from one to eight hours. The inherent poor solderability of the porous gold-plated castellation limits or prevents wetting, especially during the time frame of the 5-second immersion into liquid solder during testing. The line-scan results indicate a build-up of oxygen (nickel oxide?) in the gold plated layer after eight hours of steam ageing.

A more discerning analytical method for studying the extent to which the plated layers of the LCCC castellations actually oxidise as a function of artificial ageing would be by scanning Auger microscopy (SAM). In a recent investigation by Evans *et al*,[6] SAM, in conjunction with ion sputtering, has successfully followed the growth of oxide layers on copper plated printed circuit board terminations. The effect of ageing on oxide thickness, temperature and flux type on solderability provided an insight into the behaviour of printed circuit boards during electronic assembly processes.[6]

An IPC Task Group has undertaken a comprehensive survey of accelerated ageing techniques.[7] The suitability of any particular accelerated storage test was found to be dependent on the metallurgy of the termination and on the mechanism by which each termination was expected to degrade during actual storage conditions (e.g., by oxidation, intermetallic formation, etc.). The preferred method for accelerated ageing on tin-lead surfaces was 20 to 24 hours of steam ageing which was considered the best representation of a 1-year shelf life under normal conditions. The technical report gave no recommendations for other surface finishes. The IPC has since proposed a solderability test specification for component leads and terminations.[8] This specification differs from the Military Specification[2] in several respects, but particularly in the definition of steam ageing times: tin and tin-lead finishes require 16±1 hours whereas all other finishes require one hour of steam ageing. Only non-activated rosin flux is permitted by the IPC although other fluxes may be used for solderability testing when agreed between user and vendor.

CONCLUSIONS

1 Procurement of LCCCs supporting reflowed tin-lead terminations is to be preferred in place of gold-finished devices.

2 The assembly by tin-lead soldering of gold finished LCCC terminations is forbidden by ESA. The gold may be removed by dissolution into one liquid solder bath[4] followed by pre-tinning the terminations by dipping into a second solder bath.[4] These operations together with solder assembly onto printed circuit boards may be performed with activated soldering flux provided certain quality assurance provisions are followed (e.g., immediate removal of flux, cleanliness testing, etc.).

It is recommended that, if gold finished devices are procured, they should be stored in an inert environment such as nitrogen or argon in order to preserve solderability. Degolding and pretinning should be performed at the earliest opportunity.

3 It is recommended that solderability testing continues to be performed on all component leads and terminations according to Mil Standard 883, Test Method 2003. All devices should be steam aged for eight hours and tested with non-activated R type flux with the exception of gold finished terminals on leadless devices which may be tested with activated flux (RMA or RA).

The use of R type flux represents solder assembly processes; the use of activated flux (i.e., on gold finished LCCCs only) represents the intermediate process of degolding. All activated fluxes must be immediately cleaned off after dipping using an acceptable solvent in accordance with Reference 4.

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